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10/596,043	12/21/2006	Hassan Ihs	SC12815ET	1126

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

NOTIFICATION DATE	DELIVERY MODE
06/18/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/596,043	IHS, HASSAN	
	Examiner	Art Unit	
	HIEP NGUYEN	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The finality filed on 10-20-08 has been withdrawn in view of the Pre-Brief appeal conference decision mailed on 4/10/2009.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation " clock pulse generator apparatus comprising a clock pulse generator for generating a train of return-to zero primary clock pulses each having leading and trailing edges defining alternately an active clock phase and a non-active clock phase" is not clear. Assume the "clock pulse generator apparatus" is the circuit of figure 5. Figure 5 shows a clock pulse generator apparatus receiving "a jitter clock input signal CLK" and generates a delay clock (CLK_D) and a combined clock signal (CLK_JF). The "_train of return-to zero primary clock pulses" is not seen in figure 5 and it is not clear how it is generated. The recitations "a delay module" and "a combiner" are not clear because it is not understood whether they are separate circuits or they belong to the "clock pulse generator apparatus". The recitation "the primary clock pulse" on lines 13, 17 and 18 is confusing because it is not clear as to it is the same or different than the recitation "a train of return-to zero primary clock pulses" on line 5. It also lacks antecedent basis. The Applicant is requested to show the "train of return-to zero primary clock pulses" and the "primary clock pulse" in figure 5.

The recitation "said continuous-time sigma-delta modulator being connected to utilize said train of combined clock pulses as clock" on line 19-20 is confusing because figure 1 or figure 2 shows that the "continuous-time sigma-delta modulator" receives the "jitter clock input signal" (CLK, spec. page 7) not the train of combined clock pulses (CLK_JF) as recited. Clear explantion is required.

Regarding claim 3, the recitation "an adjustment element responsive to the said delay of said further series train of delayed clock pulses series relative to said train of primary clock pulses" on lines 9-11 is confusing because, figure 9 shows that circuit (22) receives the " jitter clock input signal" CLK and this clock is not the "said train of primary clock pulse" as recited. The recitation "said adjustment signal being averaged over a plurality of clock periods, and said adjustment signal being arranged to adjust the delay defined by said first series of delay elements" is confusing because there are different kinds of clock in the circuit of figure 9 and it is not clear whether the "plurality of clock periods" are the plurality of clock period of the " jitter clock input signal" CLK or the "further train of delay clock pulses". Clear explanation is required.

Regarding claim 4, the recitation "said delay elements" is confusing because it is not clear whether this "said delay elements" is the same or different than the "said identical delay elements" in claim 2. It also lacks antecedent basis.

Claim 5 is confusing. Claim 5 depends upon independent claim 1 which reads on figure 2. The recitation "an integrator" of claim 5 is element (2) of figure 1, the independent claim 1 reads on figure 2. The "an integrator" of claim 5 is on figure 1 and figure 1 does not have the "delay module" recited in claim 1. Clarification is required.

Regarding claim 6, the recitation "a digital-to-analog converter module whose operation is responsive to said train of combined clock pulses" is confusing because the independent claim 1 reads on figure 2. The " digital-to-analog converter module" is element (5) in figure 1. Moreover, figure 1 shows that the digital-to-analog converter module (5) whose operation is responsive to the "jitter clock input signal CLK", not the "said train of combined clock pulses" (CLK_JF) as recited. Clear explanation is required.

Claim 7 is confusing because claim 7 depends upon claim 1. Claim 1 reads on figure 2. the "input for receiving said analog signal" and "an output for said digital signal" are on figure 1.

Regarding claim 8, the recitation "wherein said continuous-time sigma-delta modulator comprises an input for receiving said digital signal and an output for said analogue signal, said digital-to-analogue -module being in series between said input and said output" is

confusing because figure 1 shows that the continuous-time sigma-delta modulator receives an analog input signal (X) and outputs a digital signal (Y).

In conclusion, claims 1-8 are indefinite because they alternately read on two distinct inventions figure 1 and figure 2. The Applicant is requested to point out which drawing is used in this application for claims 1-8. The Applicant is requested to select one of the two distinct drawings , figure 1 or figure 2. for claims 1-8.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Di Giandomenico (US 7,486,214) in view of Kim (US 7,358,786) and Tachimori (US 6,603,340).

Regarding claims 1-2, figure 1 of Di and figure 2 of Kim show an apparatus for converting between analogue and digital signals comprising:

a continuous-time sigma-delta modulator. Figure 1 of Di does not show a clock pulse generator, a delay module and a combiner. Figure 2 of Kim shows a clock pulse generator, not shown, for generating a train of return-to zero primary clock pulses (CLK) each having leading and trailing edges defining alternately an active clock phase and a non-active clock phase;

a delay module (111-115) for producing a train of delayed clock pulses presenting delayed edges whose timing relative to corresponding edges of said primary clock pulses is defined by said delay means module, and

a combiner (117) for producing a train of combined clock pulses presenting leading and trailing edges defined alternately by one of said delayed edges and the corresponding edge of the primary clock pulse, so that the active clock phases of said combined clock pulses

have widths defined by said delay module, said continuous-time sigma-delta modulator being connected to utilize said train of combined clock pulses as clock. It is obvious to one of ordinary skill in the art that because of the combiner (117), the glitch is removed thus; the variability of said widths of said active clock phases being smaller than the variability of the positions of said leading and trailing edges of said primary clock pulses, and the widths of said non-active clock phases varying as a function of variation in the positions of said primary clock pulses. The cascaded delay elements are elements 111, 113, 115.

Regarding claim 4, the combination of Di Giandomenico and Kim includes all the limitations of this claim except for the limitation that the delay elements comprise capacitive element and a current supply responsive to an input signal. Figures 2 of Tachimori shows delay elements and a current supply responsive to an input signal (Vcp, Vcn). Figure 11 shows delay element comprising capacitive element (NC1) for providing a controllable delay element capable of filtering out high frequency noise. Therefore, it would have been obvious to one of ordinary skill in the art to replace the delay element of Kim with the delay element taught by Tachimori for providing a controllable delay element capable of filtering out high frequency noise.

Regarding claim 5 and 6, the integrators are elements (54, 56, 58). The digital to analog converter is element (68).

Regarding claims 7 and 8, figures 1 and 3 of Di show that the input (IN) receives an analog signal and a feedback loop. Element (68) receives a digital input and output an analog output signal.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HIEP NGUYEN whose telephone number is (571)272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donovan D. Lincoln can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan Lam/
Primary Examiner, Art Unit 2816
/Hiep Nguyen/
Examiner, Art Unit 2816
06-14-09